Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the Application:

Listing of Claims:

1. (currently amended) A two-transistor PMOS memory cell, comprising:

a PMOS select transistor having a drain and a source formed as separate P+ diffusion regions in an N- well;

a PMOS floating gate transistor having a drain and a source formed as separate P+ diffusion regions in the N-well, wherein the P+ diffusion region that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source; and

an N implant underlying only the P+ diffusion region that forms the floating gate transistor's drain such that an N implant does not underlie either of the P+ diffusion regions forming the select ~~gate'~~ gate ~~transistor~~ transistor's drain and the floating ~~gate's~~ gate transistor's source, and wherein a lateral extent of the N implant is substantially the same as a lateral extent of the P+ diffusion region that forms the floating gate transistor's drain.

2. (cancelled)

3. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein the drain of the PMOS select transistor couples to a bit line of a memory array, and wherein a select gate of the PMOS select transistor couples to a word line of the memory array.

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4. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein a floating gate of the PMOS floating gate transistor is formed in a first polysilicon layer, and wherein a control gate of the PMOS floating gate transistor is formed in a second polysilicon layer.

5. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein the memory cell includes a single polysilicon layer containing a floating gate of the PMOS floating gate transistor, and wherein a control gate of the PMOS floating gate transistor is formed as a P+ diffusion region in the N- well.

6. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein the memory cell is configured such that the floating gate transistor may be programmed using band-to-band tunneling.

7. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein the memory cell is configured such that the floating gate transistor may be programmed using Fowler Nordheim tunneling.

8. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein the P+ diffusion region that forms the floating gate transistor's drain has a thickness of approximately 0.1 to 0.25 microns.

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9. (previously presented) The two-transistor PMOS memory cell of claim 1, wherein the thickness of the N implant underlying the P+ diffusion region that forms the

floating gate transistor's drain is approximately 0.1 to 0.25 microns.

Claims 10 – 14 (cancelled)

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